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Nodes Vs. Nodelets

Growing number of process options is creating confusion across the semiconductor industry.

JANUARY 22ND, 2018 - BY: **MARK LAPEDUS (HTTPS://SEMIENGINEERING.COM/AUTHOR/MARK-LAPEDUS/)**

Foundries are flooding the market with new nodes and different process options at existing nodes, spreading confusion and creating a variety of challenges for chipmakers.

There are full-node processes, such as 10nm and 7nm, with 5nm and 3nm in R&D. But there also is an increasing number of half-nodes or "node-lets" being introduced, including 12nm, 11nm, 8nm, 6nm and 4nm.

Node-lets are derivatives of full-node processes. For example, 12nm and 11nm are slightly more advanced versions of 16nm/14nm. And 8nm and 6nm fall under the same category as 7nm.

This becomes even less intuitive because node names don't reflect the actual physical dimensions of the transistor specs, as they did in the past. In fact, some chipmakers tout node names to show leadership position in the process race. In reality, however, these are arbitrary numbers, and many industry insiders characterize them as simply marketing terms.

Understanding the node numbers is the easy part. For foundry customers, the challenge is to decide which process to use for a design and whether it provides any value. Customers can't afford to develop a new chip for every node amid rising IC design costs. "So you have to prioritize and choose," said Wally Rhines, president and chief executive of Mentor, a Siemens Business (https://semiengineering.com/kc/entity.php?eid=22017). "You have to understand your needs and you need to understand (the foundry's) capabilities."

For foundries, the challenge is to ramp up all of these new processes. Slated for high-volume production in 2018, the new 10nm and 7nm processes are based on scaled and more complex versions of today's 16nm/14nm finFET transistors. In finFETs

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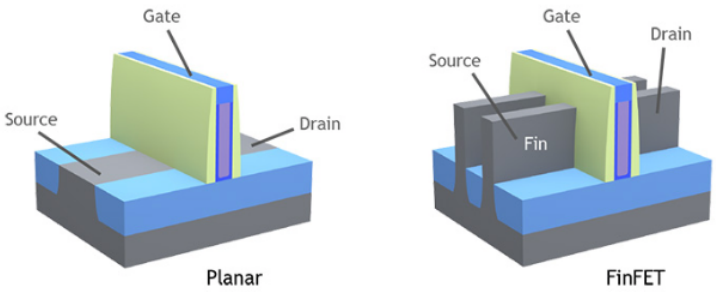

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Fig. 1: FinFET vs. planar. Source: Lam Research

The first version of 10nm/7nm will use optical lithography and multiple patterning, which introduces more mask layers and smaller feature sizes into the mix. Finding the defects is more difficult. And variation between different manufacturing equipment is becoming troublesome at 10nm/7nm.

Clearly, the industry faces some challenges. "The foundry production use of 7nm could be disappointing," said Samuel Wang, an analyst with Gartner. "My reason is that the first silicon success rate of 7nm chips by designers will be much lower than previous nodes. High design costs, design complexity, and deep collaboration requirements with partners may prevent the design of 7nm SoCs from becoming first-silicon successes in just one shot."

Over time, chipmakers are expected to iron out the problems. Then, to simplify the process, vendors hope to insert extreme ultraviolet (EUV (https://semiengineering.com/kc/technology.php?tid=31045)) lithography in the second phase of 7nm and/or at 5nm. EUV still has several challenges, however.

FinFETs are expected to scale to 5nm. Beyond that, chipmakers are working on various next-generation transistor types. Customers also are evaluating other options, such as advanced packaging.

All told, the full-node process cadence is extending from the traditional 2-year cycle to between 2.5 and 3 years. Nevertheless, with full nodes and node-lets, the industry is under pressure to deliver more and complex technologies at a faster rate. "You have nodes and inter-nodes. It doesn't matter," said Prabu Raja, senior vice president of the Semiconductor Products Group at Applied Materials (https://semiengineering.com/kc/entity.php?eid=22817). "We are in an accelerated time line. Customers are pushing us yearly with all of these changes."

What are nodes?
A chip consists of transistor and interconnects. The transistors serve as a switches. The interconnects, which reside on the top of the transistor, consist of tiny copper wiring schemes that transfer electrical signals from one transistor to another.

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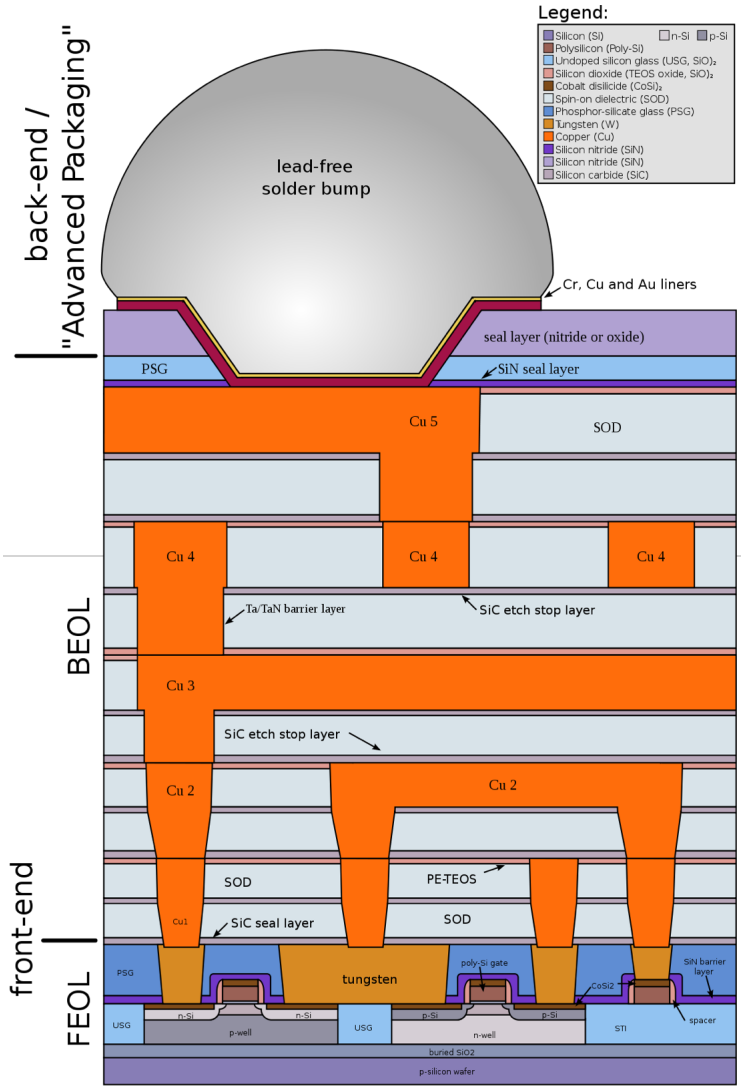

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Fig. 2: Image of chip with front-end and backend. Source: Wikipedia

Chips have 10 to 15 layers of copper interconnects. Generally, the second metal layer, called metal two (M2), has the tightest pitch. “Historically, a technology node name was based on a fraction of the tightest pitch used, typically the finest routed pitch (in M2),” said Andy Wei, an analyst at TechInsights, in a presentation.

At each node, chipmakers scaled the transistor specs by 0.7X. Using lithography techniques to shrink the transistor dimensions, the industry delivered a 15% performance boost at each node, plus a 35% cost reduction, a 50% area gain and a 40% power reduction. The formula worked as chipmakers marched down the various process nodes with numerical nanometer designations, such as 90nm, 65nm, 45nm and so on.

Things began to fall apart after 28nm, however. Intel continues to follow the 0.7X scaling trend. But at 16nm/14nm, others deviated from the traditional equation and relaxed the metal pitch. “Node names used to mean something. They used to be pinned to metal pitches,” Wei said. “At some point, we started to drift away from the pitch, focusing more on the next node and features.”

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So the node names and specs didn't correspond to the M2 pitch, and they didn't match from one vendor to the next. All told, today's node names are "more like a marketing-based number," he said. "Every single node, of course, is an improvement of the last node."

More importantly, it became more difficult to scale the transistor specs after 28nm. Lithography provided the shrinks for some but not all specs.

So, the cost-per-transistor-one key metric in scaling-no longer moved in a steep downward linear curve. "If we are tying things to actual pitches, we are getting off that line here. If we call the node name by the metal pitch divided by the actual factor, it's really flattening out and it's really not following our expectations in what we are supposed to be scaling," he said.

Moreover, fewer foundry customers could afford to move to advanced nodes amid escalating design costs. The average IC design cost for a 16nm/14nm chip is $80 million, compared to $30 million for a 28nm planar device, according to Gartner. It costs $271 million to design a 7nm chip, according to Gartner.

Moving to finFETs at 16nm/14nm became prohibitively expensive for many customers. "If customers do not need the performance of finFETs, they are not even thinking about it because it's a significant cost increase," said Walter Ng, vice president of U.S. sales at UMC (https://semiengineering.com/kc/entity.php?eid=22920). "We still see a lot of customers focused on 28nm. We see even fewer customers looking at finFETs.

Not all apps require leading-edge nodes. "If you look at automotive or IoT, a lot of these customers can't afford bleeding-edge nodes. A lot of automotive is certainly not at the bleeding edge," Ng said.

There are foundry customers that can afford the design costs at advanced nodes. They need the latest processes for traditional applications like smartphones.

The new drivers are AI, machine learning and even cryptocurrency. "The world is exploding with deep learning applications, where training requires massive computational power, usually accelerated by GPUs and special-purpose processors," said Aki Fujimura, chief executive of D2S (https://semiengineering.com/kc/entity.php?eid=22864). "That need alone will increase the world's demand on high-performance computing. So yes, absolutely there is a need to go to 7nm and beyond. GPU acceleration, in particular, is great for simulation, image processing and for deep learning. For all of these purposes, we do not have anywhere near enough compute power to do all that we want to do."

To accomplish that, the semiconductor industry can't afford to stop-or even slow down-which is why chipmakers continue to find new ways to propel chip scaling. Many of these fall under a broad category called over-scaling. Intel calls it "hyper-scaling."

For example, starting at 22nm/20nm, chipmakers began to use 193nm immersion lithography along with various multiple patterning techniques. Aimed at reducing the pitch beyond 40nm, multiple patterning involves a

process of using several lithography, etch and deposition steps in the fab.

At the same time, the structures have moved from planar to 3D. The finFET is the best example. Then, you have gate-over-contact and others. This in turn changes the materials integration mix. “When you think about going vertical, there’s a lot of new materials. How do you deposit them? How do you remove it? We see a big change the way we think about materials,” Applied’s Raja said.

Then, in another example, vendors use design technology co-optimization techniques. The idea here is to reduce the track height and cell size in a standard cell layout at each node.

Standard cells are pre-defined logic elements in a design. The cells are laid out in a grid. The track defines the height of a standard cell layout. For example, 10nm may have a 7.5-track height with a gate-pitch of 64nm and a metal pitch of 48nm, according to Imec.

Then, at 7nm, the height is reduced from 7 to 6 tracks, which results in a gate and metal pitch of 56nm and 36nm, respectively, according to Imec.

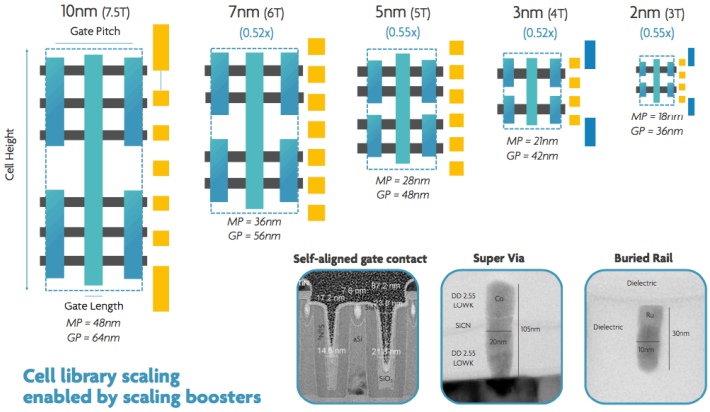

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Fig. 3: Cell library scaling enabled by scaling boosters Source: Imec

This, in turn, provides a 0.52X scaling boost. “Dimensional scaling goes hand in hand with standard cell track height scaling,” said An Steegen, executive vice president of semiconductor technology and systems at Imec (https://semiengineering.com/kc/entity.php?eid=22217). “That combination is giving you a 50% area shrink node to node.”

Starting at 14nm, Intel took it a step further by introducing a double-height track technology, where two sets of tracks are combined. “(Intel) took the original wide cell and folded it,” TechInsights’ Wei said. “On the surface, it looks like it is actually using a lot more area. It’s narrower, but it’s double the height. Folding it allows them to decrease the area. When you fold the cell, you are also using much smaller lines and able to have a lower overall resistance and higher performance.”

It’s a matter of debate whether this technique brings scaling back on the traditional cost-per-transistor curve. But this and other techniques are becoming a necessary part of the equation. “You need that, because you are adding a lot of complexity with each of these new nodes,” said Gary

Patton, chief technology officer at GlobalFoundries (https://semiengineering.com/kc/entity.php?eid=22819). "You need to over-scale. You need to scale more than 2.0X to meet the requirements."

So, what's the definition of a node and a node-let (sometimes called inter-nodes) "Full nodes, at least from an Intel perspective, need to target close to a 2X transistor density improvement compared to the previous node," explained Mark Bohr, senior fellow and director of process architecture and integration at Intel (https://semiengineering.com/kc/entity.php?eid=22846). "Full nodes are also where we typically introduce major technology changes, such as high-k/metal-gate and finFETs. Inter-nodes are where you do further optimization on that full node."

Confusing options

Regardless, foundry customers face some confusing choices. Some of the options are listed in the chart below.

Foundry	Shipping	Ramping	Readying	R&D
Intel	14nm	10nm		7nm, 5nm
GlobalFoundries	14nm		12nm, 7nm	5nm & beyond
Samsung	14nm, 10nm		11nm, 8nm, 7nm, 6nm	5nm, 4nm
TSMC	16nm, 12nm, 10nm	7nm		5nm, 3nm
UMC	14nm			Not Disclosed

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Chart 1: Foundry plans and where they are today. Source: Analysts, Foundry Reports/Semiconductor Engineering

One way to decipher the nodes is to separate Intel's strategy from others. Intel introduces a full-node process and then develops enhancements on the same process. "Intel likes to take these big steps about every three years and then do small iterations that are not too redesign-intensive," Bohr said.

Other chipmakers develop full- and half-node processes with node names that appear to be ahead of Intel. "Some of that is competitive posturing," Bohr said, adding that Intel is still ahead in the process race.

Foundries, though, are giving customers various options. Let's say 16nm/14nm is a starting point. "Some will stay at 14nm and jump straight to 7nm," GlobalFoundries' Patton said. "Some are looking for an extension of 14nm."

For example, 12nm is an extension of 16nm/14nm. It provides slightly better performance than 16nm/14nm.

At the leading edge, foundries are ramping up 10nm/7nm. Intel's 14nm process is roughly equivalent to 10nm from other foundries. Intel's 10nm is similar to 7nm from GlobalFoundries and TSMC (https://semiengineering.com/kc/entity.php?eid=22586), as well as 8nm from Samsung (https://semiengineering.com/kc/entity.php?eid=22865).

"There are four technology offerings in what I would call the '7nm zone,' " Patton explained. "We can debate who has the most density and is cheaper with the best performance. But they are all in the same zip code in PPAC."

Patton is referring to the key metrics for customers-power, performance, area and cost. So what node provides the best PPAC? As before, it largely depends on the design and application. “Foundry customers are savvy enough to know that their decisions on who and what process to use will ultimately depend on the performance of the technology, the economics and the rapport between foundry and customer,” said Joanne Itow, managing director for manufacturing at Semico Research.

One foundry customer, who spoke on the condition of anonymity, outlined one possible strategy. Generally, a company’s flagship chip product is targeted for a full-node process, such as 16nm/14nm and 7nm, according to the foundry.

Then, a company might have some derivatives or new chips slated for 16nm/14nm. For those, a company will look at the half-node processes like 12nm/11nm. “Rather than just scaling all of the layers, the foundries are scaling selected layers with these node-lets at 12nm/11nm,” according to the foundry. “So, I can go from 14nm to 11nm or something in between without adding masking layers, complexity or cost.”

12nm and/or 11nm are attractive for other reasons. In many cases, the IP is similar between 16nm/14nm and 12nm and 11nm, making it a relatively simple decision to move to these node-lets. But if the IP isn’t available at 12nm and/or 11nm, a foundry customer will avoid moving to these node-lets.

From there, customers can move to 7nm or related variants. All of this depends on the ecosystem. Not all foundries and IP houses can afford to develop IP at every node and node-let. “That complicates the adoption of node-lets. It’s not just the process technology, but the IP also needs to be there,” according to the source.

So customers must look at the entire solution. “You have to look more deeply at each process and get the specifications. A lot of things depend upon what’s important for your design in picking a process,” Mentor’s Rhines said. “It’s also important that the foundry has either physical IP you can utilize, or that you have the ability to synthesize RTL-level IP into your design and have confidence that it will work.”

On top of that, foundries need to do more handholding with customers at 7nm. “Besides making the technology ready for fab production at 7nm, foundries need to spend more time assisting design companies on design-cost reduction, IP verification and first-silicon success for fast time-to-market,” Gartner’s Wang said.

There are other considerations. Foundry customers also must examine the various processes and decide whether they fit their needs.

Not all processes are alike. But foundries are moving in similar directions at 10nm/7nm. For one thing, they are making the fins taller and thinner at each node, which in turn boosts the drive current. For instance, Intel’s 14nm finFET technology has a 42nm fin pitch and a 42nm fin height. At 10nm, Intel’s fin pitch is 34nm and the fin height is 53nm, meaning the fins are taller.

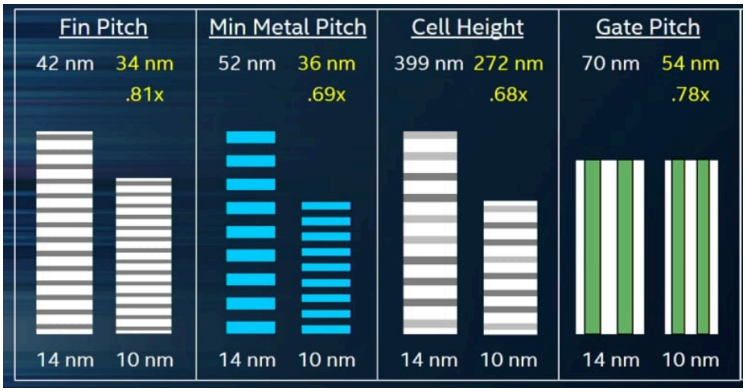

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Fig. 4: Fin, metal, gate pitches and cell height at 14nm vs. 10nm. Source: Intel

To pattern the fins and other structures, chipmakers want EUV lithography. EUV would help simplify the process, but the technology isn't ready for 10nm/7nm. So initially they will use 193nm immersion and multiple patterning for 10nm/7nm. For example, using 193nm immersion and self-aligned quadruple patterning (SAQP), Intel developed a 36nm metal pitch for its 10nm process.

Intel's 10nm process has 12 metal layers. It moved from copper to cobalt at the lowest two interconnect layers, enabling a 5-10X improvement in electromigration and a 2X reduction in via resistance.

In comparison, GlobalFoundries' 7nm finFET process has a fin pitch of 30nm, a contacted gate pitch of 56nm, and a metal pitch of 40nm. Unlike Intel, GlobalFoundries is using self-aligned double patterning for the metal layers.

"That's gives you a lot more flexibility on what you do on the backend," Patton said. "We get density in other ways. So where you have critical paths, you can go to wider lines."

GlobalFoundries' strategy also differs from Intel in the interconnect metals. "We made improvements in the copper wiring at about 100X for electromigration. So we are able to stay in copper, which has some advantages in yield and complexity," Patton said.

GlobalFoundries, though, is using cobalt for the contacts in the middle-of-line (MOL), which reduces the contact resistance.

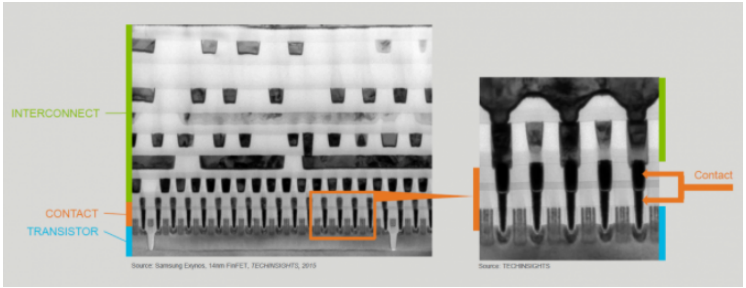

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Fig. 5: Interconnect, contact and transistor at various nodes. Source: Applied Materials.

Nevertheless, foundries face some challenges to ramp up 10nm/7nm, so customers must keep a close eye on the key issues with the technology. "The number one challenge is edge placement error. That's the combination of CD and overlay," said Ben Rathsack, senior member of the technical staff at TEL (https://semiengineering.com/kc/entity.php?eid=22940). "The middle-of-line tends to have a challenge where you are connecting your front-end to your backend. That's really where the most complexity is."

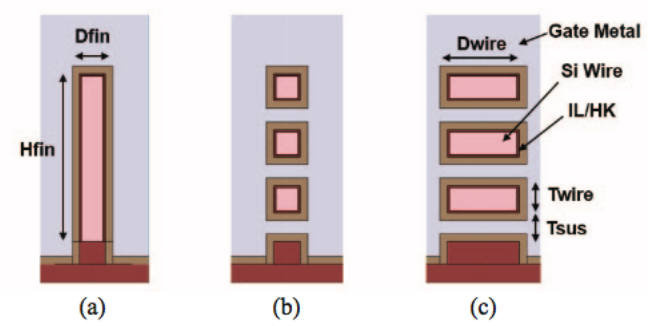
Over time, TSMC and GlobalFoundries hope to insert EUV in the second iteration of 7nm. In contrast, Samsung plans to insert EUV at 7nm in the beginning.

This depends on the readiness of EUV. "If EUV becomes mature enough that it can help reduce costs, maybe in the second or third generation of 7nm, then that implementation could happen," Rathsack said.

What's next?

It's unclear if all of the node names will stick in the long run. A bigger question is how far will the finFET scale? "The path to 5nm is pretty clear. FinFETs will get extended at least to 5nm. It's possible they will get extended to 3nm," said Rick Gottscho, CTO at Lam Research (https://semiengineering.com/kc/entity.php?eid=22820). "And there will be some other solutions after that, whether that's gate-all-around horizontally or vertically. There will be new materials. There also will be a lot of challenges."

The industry is exploring the lateral gate-all-around FET and the nanosheet FET. In both cases, a finFET is placed on its side and a gate wraps around it.



(https://semiengineering.com/wp-content/uploads/2018/01/pic6.png)

Fig. 6: Cross-section simulation of (a) finFET, (b) nanowire, and (c) nanosheet. Source: IBM

It's too early to say what will happen at 5nm and beyond. "5nm device structures are still undetermined by some foundries. It seems as if TSMC and GF will use finFETs. Samsung may choose gate-all-around for 5nm (and 4nm). Intel is still unknown at this time," Gartner's Wang said. "Until there are some success stories on 7nm with EUV in production, I do not believe designers are wise to commit to 5nm."

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